ABSTRACT OF THE DISCLOSURE

A method, system and protocol for a synchronous memory system. One embodiment of a system comprises: a memory control device; one or more memory modules in a main memory, with each memory module comprising one or more memory banks; a transfer bus for communication between the memory control device and the memory modules, where the transfer bus is in the form of a concatenated bus structure and comprises a plurality of parallel transfer lines; and where the memory control device is designed to generate commands comprising a plurality of command segments with a respective plurality of elements, and to transfer them to the memory modules using the transfer bus. The transfer bus is configured to transfer the elements of a command segment in parallel, and the commands each comprise a selection command segment for selecting one or more memory banks, with each of the memory banks having at least one uniquely associated element of the selection command segment.

254608_1.DOC